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DESIGN NOTE #025

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SPI Setup and Hold Times

Introduction

This document explains why SPI Setup and Hold Times are of no concern to the system designer, as long as the SPI Master operates in the mode expected by the Slave.

Overview

The Serial Peripheral Interface (SPI) bus is designed to provide very high communication speeds between devices on the same PCB. To maximize its flexibility and ensure correct operation even in the most complex designs, the SPI assigns the Setup and Sample operation to alternate clock edges of the SCK clock.

Clock Phase and Polarity

CPHA

The settings of the Clock Phase bit (CPHA) determine if data is sampled on the leading (first) or trailing (last) edge of SCK.

Table 1. The Effect of CPHA Settings

	Leading Edge	Trailing Edge
CPHA = 0	Sample	Setup
CPHA = 1	Setup	Sample

CPOL

The settings of the Clock Polarity bit (CPOL) determine if the first clock edge of SCK is a rising (low-to-high) or a falling (high-to-low) edge.

Table 2. The Effect of CPOL Settings

	Leading Edge	Trailing Edge
CPOL = 0	Rising	Falling
CPOL = 1	Falling	Rising

Combining the two tables above into one table is shown in Table 3.

Table 3. The Combined Effect of CPHA and CPOL Settings

	Leading Edge	Trailing Edge	SPI Mode
CPOL = 0, CPHA = 0	Sample (rising)	Setup (falling)	Mode 0
CPOL = 0, CPHA = 1	Setup (rising)	Sample (falling)	Mode 1
CPOL = 1, CPHA = 0	Sample (falling)	Setup (rising)	Mode 2
CPOL = 1, CPHA = 1	Setup (falling)	Setup (rising)	Mode 3

Setup and Hold Times

Figure 1 and Figure 2 illustrate how data on both MOSI and MISO is set up and sampled on opposite edges of the SPI clock SCK. Data is set up half a clock period before the sampling edge. Data is held half a period after the sampling edge.

Figure 1. Mode 0 and Mode 2 sample data on the leading edge of SCK (CPHA = 0)

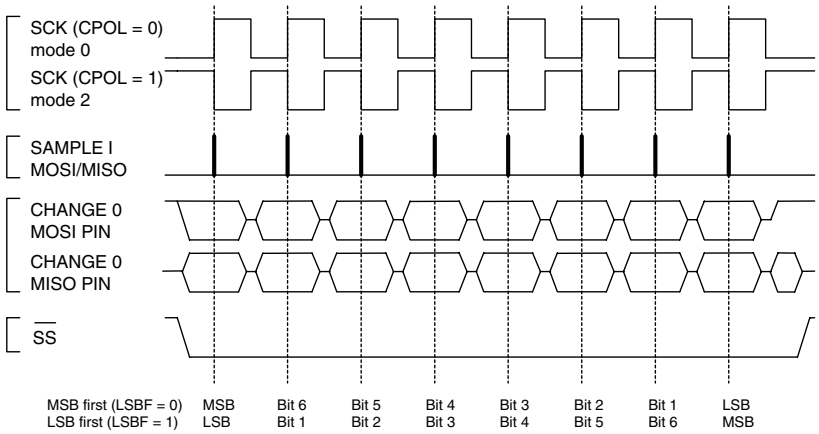

Figure 2. Mode 1 and Mode 3 sample data on the trailing edge of SCK (CPHA = 0)